B.Tech. DEGREE EXAMINATION, NOVEMBER 2017

Third/Fourth/Fifth Semester

15EC325E – DIGITAL LOGIC DESIGN WITH PLDS AND VHDL

(For the candidates admitted during the academic year 2015 – 2016 onwards)

Note:

(i) **Part - A** should be answered in OMR sheet within first 45 minutes and OMR sheet should be handed over to hall invigilator at the end of 45th minute.

(ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: Three Hours | Max. Marks: 100

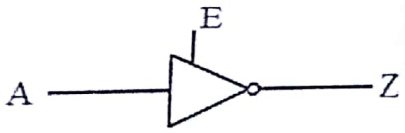
PART – A (20 × 1 = 20 Marks)

Answer **ALL** Questions

1. The logical expression $ab\bar{c}\bar{d} + abc\bar{d}$ is equivalent to
   (A) abd (B) ab
   (C) $ab\bar{d}$ (D) $a\bar{d}$

2. How many select lines are required to make a 64×1 multiplexer?
   (A) 2 (B) 4
   (C) 6 (D) None

3. Identify the output state of the tri-state inverter shown below. When $A = 0,\ E = 0,\ Z = ?$



   (A) 0 (B) Hi-Z
   (C) 1 (D) "X"

4. The output of the circuit is always

   (A) A (B) $\bar{A}$
   (C) 1 (D) 0

5. If the JK flipflop can be operated as a toggle flipflop. Apply a 10 kHz clock signal and determine the frequency of Q output.
   (A) 5 kHz square wave (B) 10 kHz square wave
   (C) 20 kHz square wave (D) None

6. The characteristic equation for SR flip flop is
   (A) $Q_{n+1} = \bar{S}Q + R$ (B) $Q_{n+1} = \bar{S}Q + \bar{R}Q$
   (C) $Q_{n+1} = S + Q\bar{R}$ (D) $Q_{n+1} = SQ + R$

7. The content of a 4-bit register is initially 1101. The register is shifted 6 time to the right with serial input being 101101. What is the content of the register after each shift?
   (A) (1101;1111;0011;1010;0101;1111)
   (B) (1110;0111;1011;1101;0110;1011)
   (C) (1111;1101;1001;1110;1111;1010)
   (D) (0001;0010;0011;0100;0101;0110)

8. For Mealy circuit
   (A) The output depends on both the present state and present inputs
   (B) The output depends on either present state or present inputs
   (C) The output depends on both the present state and clock inputs
   (D) The output depends only on present state

9. CPLD is an acroym for
   (A) Computer Programmable Logic Device
   (B) Complement Programmable Logic Device
   (C) Complex Programmable Logic Device
   (D) CMOS Programmable Logic Device

10. The content of a simple PLD's consists of
   (A) Fuse link arrays
   (B) Thousand of basic logic gates
   (C) Advanced sequential logic function
   (D) Thousand of basic logic gates and advanced sequential logic function

11. The storage element for a static RAM is
   (A) Diode
   (B) Resistor
   (C) Capacitor
   (D) Flipflop

12. The number of CLB's available in Xilinx XC303A, 3030L, 3130A
   (A) 144
   (B) 120
   (C) 96
   (D) 100

13. In VHDL, which object are used to connect entities together for the model formation?
   (A) Constant
   (B) Variable
   (C) Signal
   (D) All of the above

14. The default range of integer data types supported in VHDL
   (A) – 2, 647,483,147 to +2,647,483,147
   (B) –2,147,483,647 *to* + 2,147,483,647
   (C) – 2,483,147,647 to +2,483,147,647
   (D) – 2.147,647,483 to +2,147,647,483

15. An anti fuse programming technology is predominantly associated with _____
   (A) CPLDs
   (B) SPLDs
   (C) FPGAs
   (D) All of the above

16. Find *x, y* when a = 0001, b = 1001, c = 1100. [note: *x* is the inout bit vector]
   Architecture ar of oa is
   Begin
   x⇐ a and b; y = *x* or c;
   end ar;
   (A) 1101, 1100
   (B) 1100, 1101
   (C) 1101, 0001
   (D) 0001,1101

17. Identify the following program
entity find is port (a, b, c, d: in bit; x, y, w, z: out bit);
end find;
architecture ar of find is begin
x<= a; y<= a xor b; w<= b xor c; z<= c xor d;
end ar;
(A) Binary to gray code converter (B) Gray to binary code converter
(C) Binary to excess-3 converter (D) Excess-3 to binary converter

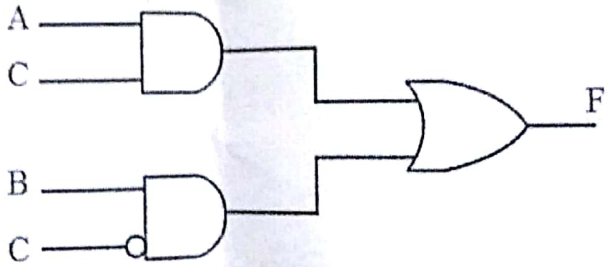
18. Determine the number of flip flop that would be required to build the following counters: mod-6, mod-11, mod-15, mod-19, mod-31.
(A) 2,4,4,5,5 (B) 3,5,5,4,4
(C) 3,4,4,5,5 (D) 5,5,3,4,4

19. Find the value of y, when a = 1111, b = 1111 architecture mul of twoip is
Begin
y <= a *b;
end mul;
(A) 11100001 (B) 11000011
(C) 10000010 (D) 11111100

20. Find the value of SO? When DI = 01010101. [Note: S is the inout unsigned vector]
architecture ar of shifting is
begin S <= DI rol 1; SO <= S ror 3;
end ar;
(A) 010101xx (B) Xx101010
(C) 01010101 (D) 10101010

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

21. Define: Hazard. Eliminate the static "1" hazard for the given circuit.



22. With the state diagram as example, list the difference between Mealy and Moore circuit.

23.i. Write a short notes on PROM.

ii. Implement the Boolean function using PAL $F = \Sigma m(2,12,13)$.

24. List the types of operator available in VHDL and explain any two.

25. Explain the package in VHDL.

26. Write a VHDL code for D-flip flop.

27. Design a single bit comparator and write the VHDL code for the same.

PART – C (5 x 12 = 60 Marks)
Answer **ALL** Questions

28. a.i. Explain Reed Muller expansion theorem with an example. (4 Marks)

ii. By applying the Shannon's expansion theorem implement the following function using one 2×1 multiplexer and logic gates. $F = X'Y'Z' + X'Y'Z' + X'YZ + XY'Z' + XY'Z$. (8 Marks)

(OR)

b.i. Simplify the following Boolean equation and eliminate the consensus terms.
$F_1 = A'C' + ABD + BC'D + AB'D' + ABCD'$
$F_2 = A'B + ABD + AB'CD' + BC$

ii. With the design example, explain how multiplexer is working as logic function generator.

29. a. A sequential circuit has one input (X) and one output (Z). The circuit produces an output Z=1 for the input sequence 101. Find the Mealy state graph and design the circuit using D-flip flop.
$X = 0011011001010100$
$Z = 0000010000010100$

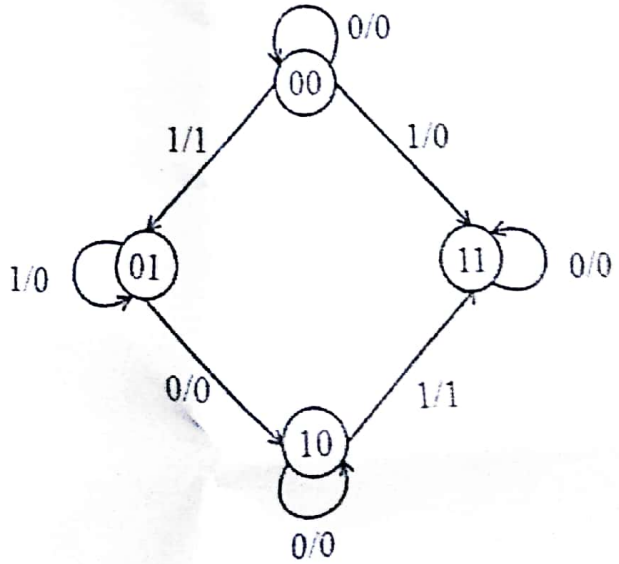
(OR)

b. Design a synchronous 3-bit gray code up-counter using JK flip flops.

30. a. With a neat sketch explain the Xilinx 4000 architecture.

(OR)

b. Design the synchronous sequential circuit for the given state diagram with D-flip flop and implement using PAL16R6.



31. a.i. What is an entity in VHDL? (3 Marks)

ii. What is the significance of architecture declaration in VHDL? (3 Marks)

iii. Define process statement and list its types and explain any two. (6 Marks)

(OR)

b.i. Explain the different types of data objects present in VHDL.

ii. Distinguish between concurrent and sequential signal assignment with example.

32. a. Develop a VHDL program for BCD adder using full adders and logic gates as a component.

(OR)

b.i. Write a VHDL program for 3×8 decoder with enable input in dataflow modeling.

ii. Write a VHDL program for 4-bit up/down counter in behavioral modeling.

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